

December 1993

10-Bit, 12-Bit Multiplying D/A Converters

Features

- AD7520/AD7530 10 Bit Resolution; 8, 9 and 10 Bit Linearity
- AD7521/AD7531 12 Bit Resolution; 8, 9 and 10 Bit Linearity
- Low Power Dissipation of 20mW (Max)
- Low Nonlinearity Tempco at 2ppm of FSR/°C
- Current Settling Time 1.0μs to 0.05% of FSR
- ±5V to +15V Supply Voltage Range
- TTL/CMOS Compatible
- Full Input Static Protection
- /883B Processed Versions Available

Description

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

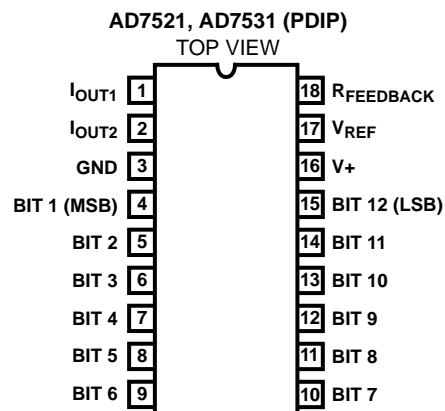
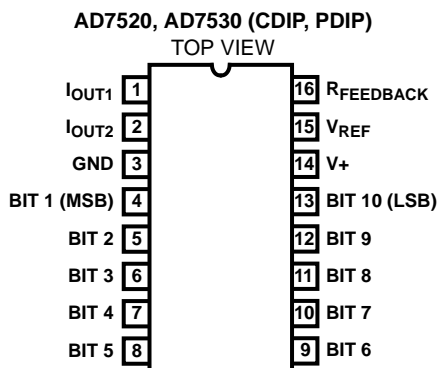
Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

Ordering Information

PART NUMBER	NONLINEARITY	TEMPERATURE RANGE	PACKAGE
AD7520JN, AD7530JN	0.2% (8-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7520KN, AD7530KN	0.1% (9-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7521JN, AD7531JN	0.2% (8-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7521KN, AD7531KN	0.1% (9-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7520LN, AD7530LN	0.05% (10-Bit)	-40°C to +85°C	16 Lead Plastic DIP
AD7521LN, AD7531LN	0.05% (10-Bit)	-40°C to +85°C	18 Lead Plastic DIP
AD7520JD	0.2% (8-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520KD	0.1% (9-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520LD	0.05% (10-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520SD, AD7520SD/883B	0.2% (8-Bit)	-55°C to +125°C	16 Lead Ceramic DIP
AD7520TD	0.1% (9-Bit)	-55°C to +125°C	16 Lead Ceramic DIP
AD7520UD, AD7520UD/883B	0.05% (10-Bit)	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts



Specifications AD7520, AD7530, AD7521, AD7531

Absolute Maximum Ratings

Supply Voltage (V+ to GND).....	+17V
V _{REF}	±25V
Digital Input Voltage Range	V+ to GND
Output Voltage Compliance	-100mV to V+
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10s).....	300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Plastic DIP	100°C/W	-
18 Lead Plastic DIP	90°C/W	-
16 Lead Ceramic DIP	80°C/W	24°C/W
Maximum Power Dissipation		
Up to +75°C.....	450mW	
	Derate Above +75°C at 6mW/°C	
Operating Temperature		
JN, KN, LN Versions	0°C to +70°C	
JD, KD, LD Versions	-25°C to +85°C	
SD, TD, UD Versions	-55°C to +125°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FEEDBACK}.

Electrical Specifications V+ = +15V, V_{REF} = +10V, T_A = +25°C Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
SYSTEM PERFORMANCE (Note 1)									
Resolution		10	10	10	12	12	12	Bits	
Nonlinearity	J, S	S Over -55°C to +125°C (Notes 2, 5) (Figure 2)		-	-	±0.2 (8-Bit)	-	±0.2 (8-Bit)	% of FSR
	K, T	T Over -55°C to +125°C (Figure 2)		-	-	±0.1 (9-Bit)	-	±0.1 (9-Bit)	% of FSR
	L, U	-10V ≤ V _{REF} ≤ +10V U Over -55°C to +125°C (Figure 2)		-	-	±0.05 (10-Bit)	-	±0.05 (10-Bit)	% of FSR
Nonlinearity Tempco	-10V ≤ V _{REF} ≤ +10V (Notes 2, 3)		-	-	±2	-	-	±2	ppm of FSR/°C
Gain Error			-	±0.3	-	-	±0.3	-	% of FSR
Gain Error Tempco			-	-	±10	-	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)	Over the Specified Temperature Range		-	-	±200 (±300)	-	-	±200 (±300)	nA
DYNAMIC CHARACTERISTICS									
Output Current Settling Time	To 0.05% of FSR (All Digital Inputs Low To High And High To Low) (Note 3) (Figure 7)		-	1.0	-	-	1.0	-	µs
Feedthrough Error	V _{REF} = 20V _{p-p} , 10kHz (50kHz) All Digital Inputs Low (Note 3) (Figure 6)		-	-	10	-	-	10	mV _{p-p}
REFERENCE INPUT									
Input Resistance	All Digital Inputs High I _{OUT1} at Ground		5	10	20	5	10	20	kΩ
ANALOG OUTPUT									
Output Capacitance	I _{OUT1}	All Digital Inputs High (Note 3) (Figure 5)	-	200	-	-	200	-	pF
	I _{OUT2}		-	75	-	-	75	-	pF
	I _{OUT1}	All Digital Inputs Low (Note 3) (Figure 5)	-	75	-	-	75	-	pF
	I _{OUT2}		-	200	-	-	200	-	pF

Specifications AD7520, AD7530, AD7521, AD7531

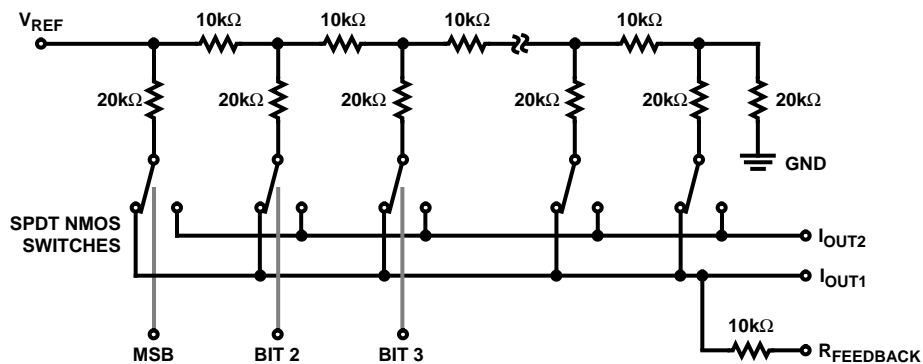
Electrical Specifications $V_+ = +15V$, $V_{REF} = +10V$, $T_A = +25^\circ C$ Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Noise	Both Outputs (Note 3) (Figure 4)	-	Equivalent to 10k Ω	-	-	Equivalent to 10k Ω	-	Johnson Noise
DIGITAL INPUTS								
Low State Threshold, V_{IL}	Over the Specified Temperature Range $V_{IN} = 0V$ or $+15V$	-	-	0.8	-	-	0.8	V
High State Threshold, V_{IH}		2.4	-	-	2.4	-	-	V
Input Current, I_{IL} , I_{IH}		-	-	± 1	-	-	± 1	μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary						
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection	$V_+ = 14.5V$ to $15.5V$ (Note 2) (Figure 3)	-	± 0.005	-	-	± 0.005	-	% FSR/% ΔV_+
Power Supply Voltage Range		+5 to +15			+5 to +15			V
I_+	All Digital Inputs at 0V or V_+ Excluding Ladder Network	-	± 1	-	-	± 1	-	μA
	All Digital Inputs High or Low Excluding Ladder Network	-	-	2	-	-	2	mA
Total Power Dissipation	Including the Ladder Network	-	20	-	-	20	-	mW

NOTES:

1. Full scale range (FSR) is 10V for Unipolar and $\pm 10V$ for Bipolar modes.
2. Using internal feedback resistor $R_{FEEDBACK}$.
3. Guaranteed by design, or characterization and not production tested.
4. Accuracy not guaranteed unless outputs at GND potential.
5. Accuracy is tested and guaranteed at $V_+ = 15V$ only.

Functional Diagram



Switches shown for Digital Inputs "High".
Resistor values are typical.

Test Circuits The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

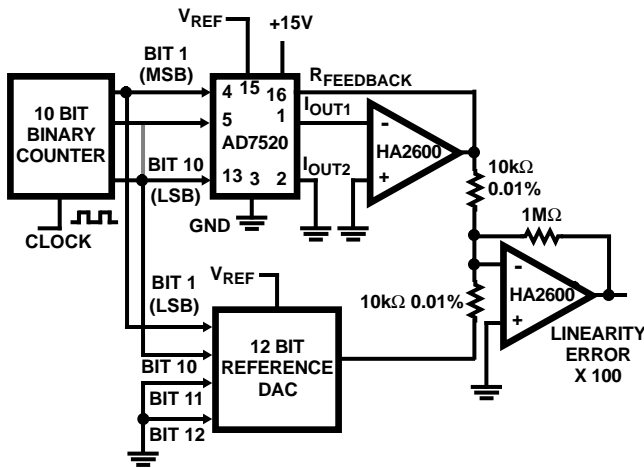


FIGURE 2. NONLINEARITY

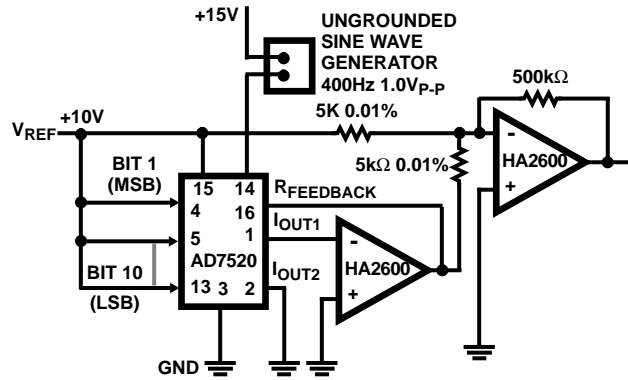


FIGURE 3. POWER SUPPLY REJECTION

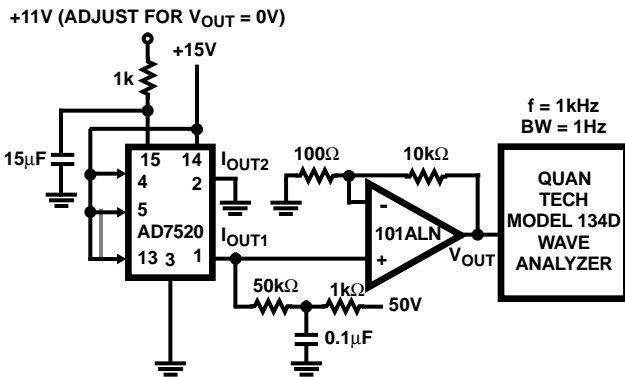


FIGURE 4. NOISE

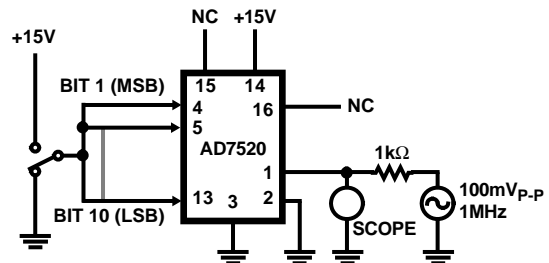


FIGURE 5. OUTPUT CAPACITANCE

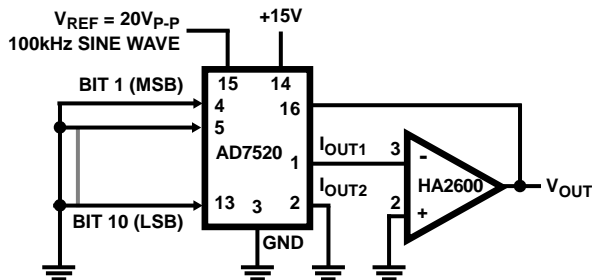


FIGURE 6. FEEDTHROUGH ERROR

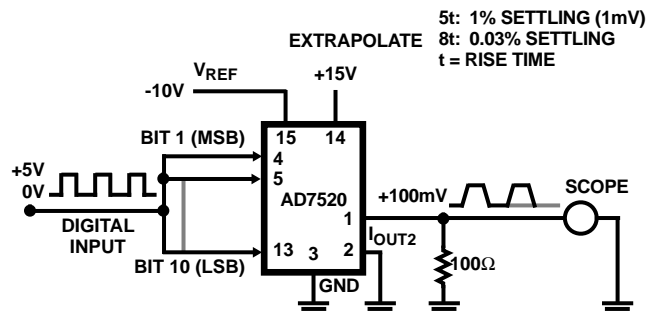


FIGURE 7. OUTPUT CURRENT SETTLING TIME

5t: 1% SETTling (1mV)
8t: 0.03% SETTling
t = RISE TIME

Applications

Unipolar Binary Operation

The circuit configuration for operating the AD7520 in unipolar mode is shown in Figure 8. Similar circuits can be used for AD7521, AD7530 and AD7531. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

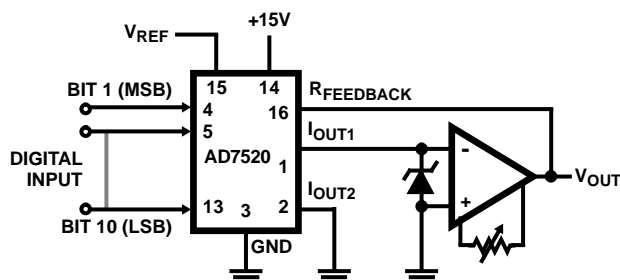


FIGURE 8. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

TABLE 1. CODE TABLE - UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF} (1-2^{-N})$
1000000001	$-V_{REF} (\frac{1}{2} + 2^{-N})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF} (\frac{1}{2} - 2^{-N})$
0000000001	$-V_{REF} (2^{-N})$
0000000000	0

NOTES:

1. $LSB = 2^{-N} V_{REF}$
2. $N = 10$ for 7520, 7530
 $N = 12$ for 7521, 7531

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V at V_{OUT} .

Gain Adjustment

1. Connect all digital inputs to $V+$.
2. Monitor V_{OUT} for a $-V_{REF} (1-2^{-N})$ reading. ($N = 10$ for AD7520/30 and $N = 12$ for AD7521/31).
3. To decrease V_{OUT} , connect a series resistor (0 to 250 Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT} , connect a series resistor (0 to 250 Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 in the bipolar mode is given in Figure 9. Similar circuits can be used for AD7521, AD7530 and AD7531. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The

"Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

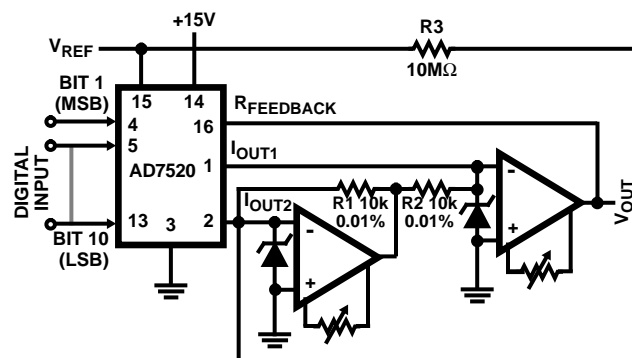


FIGURE 9. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

TABLE 2. BIPOLAR (OFFSET BINARY) CODE TABLE

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF} (1-2^{-(N-1)})$
1000000001	$-V_{REF} (2^{-(N-1)})$
1000000000	0
0111111111	$V_{REF} (2^{-(N-1)})$
0000000001	$V_{REF} (1-2^{-(N-1)})$
0000000000	V_{REF}

NOTES:

1. $LSB = 2^{-(N-1)} V_{REF}$
2. $N = 10$ for 7520, 7521
 $N = 12$ for 7530, 7531

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10M Ω), from V_{REF} to I_{OUT2} .

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V \pm 1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V \pm 1mV at V_{OUT} .

Gain Adjustment

1. Connect all digital inputs to $V+$.
2. Monitor V_{OUT} for a $-V_{REF} (1-2^{-(N-1)})$ volts reading. ($N = 10$ for AD7520 and AD7530, and $N = 12$ for AD7521 and AD7531).
3. To increase V_{OUT} , connect a series resistor of up to 250 Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT} , connect a series resistor of up to 250 Ω between the reference voltage and the V_{REF} terminal.

AD7520, AD7530

Die Characteristics

DIE DIMENSIONS:

101 x 103mils (2565 x 2616micrms)

METALLIZATION:

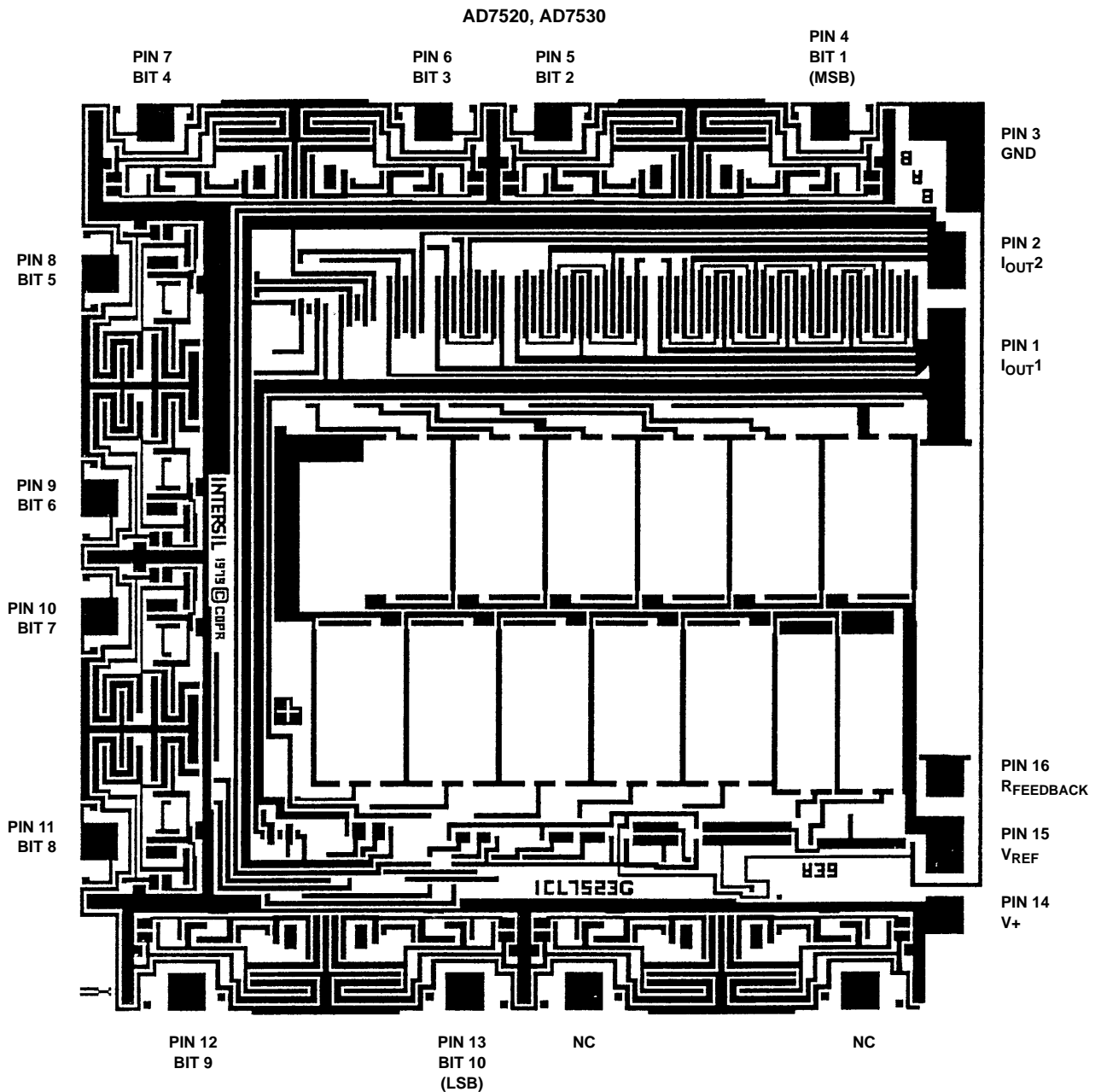
Type: Pure Aluminum
Thickness: $10 \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: PSG/NITRIDE
PSG: $7 \pm 1.4\text{k}\text{\AA}$
NITRIDE: $8 \pm 1.2\text{k}\text{\AA}$

PROCESS: CMOS Metal Gate

Metallization Mask Layout



AD7521, AD7531

Die Characteristics

DIE DIMENSIONS:

101 x 103mils (2565 x 2616micrms)

METALLIZATION:

Type: Pure Aluminum
Thickness: $10 \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: PSG/NITRIDE
PSG: $7 \pm 1.4\text{k}\text{\AA}$
NITRIDE: $8 \pm 1.2\text{k}\text{\AA}$

PROCESS: CMOS Metal Gate

Metallization Mask Layout

